

Remarks:

Reconsideration of the application is requested.

Claims 1-11 remain in the application. Claim 7 has been amended. Claims 7-11 have withdrawn from consideration in view of the restriction requirement made by the Examiner in the Office action dated July 9, 2002.

The Examiner is requested to re-consider the restriction requirement made in the Office action dated July 9, 2002. On page 2 of the Office action dated July 9, 2002, the Examiner stated as the reason for the restriction requirement that "[i]n the instant case the hole of the device can be formed by laser ablating or by mechanical drilling and thus forming the device with a materially different method." Applicant reviewed independent product claim 1 and independent method claim 7, and by amending claim 7 to recite "**forming** a contact hole" instead of "etching a contact hole" it is believed that the reason for the restriction requirement is overcome.

In the fourth paragraph on page 2 of the above-identified Office action, the title has been held as not being (sufficiently) descriptive. Accordingly, a new title -  
INTEGRATED CIRCUIT CONFIGURATION USING SPACERS AS A DIFFUSION  
BARRIER AND METHOD OF PRODUCING SUCH AN INTEGRATED CIRCUIT

CONFIGURATION - is proposed, and the entry thereof is requested.

In the fifth paragraph on page 2 of the Office action, the disclosure has been objected to and the Examiner has stated that "[t]he related application information should be updated." The appropriate corrections have been made to the instant application.

In the sixth paragraph on page 2 of the Office action, claims 1-6 have been rejected as being indefinite under 35 U.S.C. § 112, second paragraph.

More specifically, the Examiner has stated that, according to the drawings, there is an electrical connection between the first conductive structure and the second conductive structure only "if the second diffusion layer is an electrically conductive layer. If this is the case, why is it called a diffusion barrier layer?" The layer mentioned by the Examiner is recited in claim 4 as an "**electrically** conductive second diffusion barrier structure" (emphasis added) "acting as a barrier to diffusion of material from said second conductive structure." It is believed that the omission of the feature "electrically second diffusion barrier structure" does not render claim 1 incomplete for omitting essential matter under MPEP § 2172.01 (8<sup>th</sup> edition). Therefore, Applicant believes

that it is not necessary to amend claim 1 to overcome the § 112 rejection.

It is accordingly believed that the specification and the claims meet the requirements of 35 U.S.C. § 112, second paragraph. Should the Examiner find any further objectionable items, Counsel would appreciate a telephone call during which the matter may be resolved.

In the first paragraph on page 4 of the Office action, claims 1-6 have been rejected as being anticipated by Inohara et al. (US 5,966,634) under 35 U.S.C. § 102.

In the second paragraph on page 4 of the Office action, claims 1-6 have been rejected as being anticipated by Mu et al. (US 5,612,254) under 35 U.S.C. § 102.

In the third paragraph on page 4 of the Office action, claims 1-6 have been rejected as being anticipated by Nguyen (EP 0 892 428) under 35 U.S.C. § 102.

As will be explained below, it is believed that the claims were patentable over the cited art in their original form and the claims have, therefore, not been amended to overcome the references.

Before discussing the prior art in detail, it is believed that a brief review of the invention as claimed, would be helpful.

Claim 1 calls for, inter alia:

an insulating layer;

a first conductive structure embedded in said insulating layer;

a diffusion barrier layer and a second insulating layer disposed above said first conductive structure and being formed with a contact hole reaching as far as said first conductive structure and having side walls;

a second conductive structure disposed in said contact hole and conductively connected to said first conductive structure; and

spacers formed on said side walls of said contact hole above said diffusion barrier layer, **said spacers acting as a barrier to diffusion of a material from said first conductive structure into said second insulating layer** and reaching as far as a surface of said diffusion barrier layer.

The inventive concept of the invention of the instant application the avoidance of the diffusion of material from a first conductive structure into a second conductive structure by using "spacers" acting as a diffusion barrier (see the paragraph bridging pages 4-5 of the instant application).

Below is a discussion of the applied references and whether or not the applied references disclose or suggest such a "spacer".

***Inohara et al.* (US 5,966,634)**

*Inohara et al.* state at col. 14, line 62, through col. 15, line 13:

Next, as shown in FIG. 15, a copper diffusion preventing film 765 whose thickness is 50 nm comprising the silicon nitride is formed by using the sputter method or the CVD method.

Next, as shown in FIG. 16, the copper diffusion preventing film 765 portion of an connecting hole bottom portion 775 is etching-removed by using the anisotropic etching method without using the mask. In this case, the upper surface of the interlayered insulating film 740 and the ***copper diffusion preventing film 765*** portion of an wiring groove bottom portion 770 are also simultaneously ***removed***. In the wiring groove bottom portion 770, since the etching stopper film 735 exists, the interlayered insulating film 730 is not exposed. Furthermore, thereafter, the metal wire material having the main component of the copper or containing the pure copper is embedded in the connecting holes 760, 755 and the wiring groove 745. Thereby, the semiconductor device having the multi-layer wire structure is manufactured.

(emphasis added)

The above-noted passage of *Inohara et al.* contains the only mention of the copper diffusion preventing film 765. Because the copper diffusion preventing film 765 is removed, it is believed that *Inohara et al.* do not disclose a circuit having

spacers acting as a diffusion barrier, as recited in the claims of the instant application.

**Mu et al. (US 5,612,254)**

Mu et al. state in col. 7, lines 65, through col. 8, line 3, that:

The copper within the interconnects is encapsulated to prevent copper diffusion into a silicon dioxide layer. FIG. 8 illustrates the copper being surrounded by the **titanium nitride barrier layer 60** and the silicon oxynitride passivation layer 80. Titanium nitride and silicon oxynitride act as **diffusion barriers to the copper**.

(emphasis added)

The titanium nitride barrier layer 60 of Mu et al. apparently has the function of preventing diffusion of material from the copper disposed in a contact hole ("**second** conductive structure") into the silicon dioxide layer (the "second insulation layer"). However, the claims of the instant application state that the spacers act as a barrier to diffusion of a material from the conductive structure embedded in the insulating layer ("**first** conductive structure") into the insulating layer. Consequently, it is believed that Mu et al. do not read on the claims of the instant application.

**Nguyen (EP 0 892 428)**

The instant application claims a priority date of September 23, 1998. The applied reference Nguyen (EP 0 892 428) has a date of publication of January 20, 1999, and therefore would not be available against the instant application once the claim for priority has been perfected. However, Nguyen (EP 0 892 428) claims the priority of a US patent application which was granted as US Patent No. 5,904,565 and No. 6,023,102.

Consequently, although Nguyen (EP 0 892 428) would not be available as prior art once the claim for priority would have been perfected, the corresponding Nguyen (US 5,904,565 and 6,023,102) would be available as prior art.

Regarding the "vertical sidewall surfaces 202" and the "sixth barrier layer 214", Nguyen (EP 0 892 428) only contains the following disclosure:

Paragraph between col. 11, line 53, and col. 12, line 9, states:

FIG. 18 is a partial cross-sectional view of IC 160 wherein a CMP is performed on second metal level 188. In some aspects of the invention, the CMP process also removes second barrier layer 178 overlying first dielectric interlevel 166. IC 160 further comprises a fourth barrier layer 190 overlying second metal level 188, and a second dielectric interlevel 192 overlying fourth barrier layer 190. Second dielectric interlevel 192 has a first thickness 194 and a second thickness 196 overlying first thickness 194. A second damascene via 200 through selected overlying areas of fourth barrier layer 190 and second dielectric interlevel first

thickness 194 exposes **vertical sidewall surfaces 202** of second dielectric interlevel first thickness 194 and selected areas 204 of second metal level 188.

(emphasis added)

Paragraph in col. 12, lines 24-44, states:

IC 160 also comprises an **sixth barrier layer 214** formed by conformally depositing **sixth barrier layer 214** over **vertical sidewall surfaces 202** of first dielectric interlevel first thickness 194 and vertical sidewall surfaces 208 of second dielectric interlevel second thickness 196, and second metal level selected areas 204. Typically in this process, fifth barrier layer 212, covering selected horizontal surfaces 210 of second dielectric interlevel first thickness 194, is also conformally coated with **sixth barrier layer 214**. **Sixth barrier layer 214** is then anisotropically etched, in the horizontal direction, to selectively remove **sixth barrier layer 214** deposited over second metal level selected areas 204. In this etching process, **sixth barrier layer 214** is removed from fifth barrier layer 212 covering selected horizontal surfaces 210 of second dielectric interlevel first thickness 194, and fifth barrier layer 212 overlying second dielectric interlevel 192. Second via 200 and second trench 206 have barrier **sidewall surfaces 214**, and are prepared to directly connect second metal level 188 with a subsequently deposited metal level (not shown).

(emphasis added)

There is no express or implied disclosure in *Nguyen* of a "spacer" as recited in the claims of the instant application. It is also doubtful whether there is an inherent disclosure of a "spacer" in *Nguyen*. Consequently, it is believed that *Nguyen* does not read on the claims of the instant application.

Clearly, neither *Inohara et al.*, *Mu et al.*, nor *Nguyen* show a "spacer" as recited in claims 1 and 7 of the instant application. Therefore, the invention as recited in claims 1 and 7 of the instant application is believed not to be anticipated by either one of *Inohara et al.*, *Mu et al.*, or *Nguyen*.

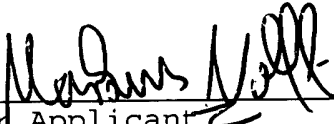
It is accordingly believed to be clear that none of the applied references shows the features of claims 1 and 7. Claims 1 and 7 are, therefore, believed to be patentable over the art and because claims 2-6 and 8-11 are ultimately dependent on claims 1 and 7, respectively, they are believed to be patentable as well.

In view of the foregoing, reconsideration and allowance of claims 1-11 are solicited.

Petition for extension is herewith made. The extension fee for response within a period of one month pursuant to Section 1.136(a) in the amount of \$ 110.00 in accordance with Section 1.17 is enclosed herewith.

Please charge any other fees which might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner and Greenberg, P.A., No. 12-1099.

Respectfully submitted,

  
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For Applicant

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~~December 13, 2002~~ Jan 10, 2003

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Applic. No. : 09/816,923

Version with markings to show changes made:

Page 1, lines 6-8, with -

This application is a continuation of copending International Application No. PCT/DE99/02927, filed September 14, 1999, which designated the United States and which was not published in the English language. -

Claim 7 (amended). A method of producing an integrated circuit configuration, which comprises:

forming a diffusion barrier layer on a substrate having at least a first insulating layer with a first conductive structure embedded therein;

forming a second insulating layer on the diffusion barrier layer;

[etching] forming a contact hole into the second insulating layer above the first conductive structure, wherein the surface of the first conductive structure is covered with the diffusion barrier layer within the hole;

forming spacers on side walls of the contact hole, the spacers acting as a barrier to diffusion of a material from the first conductive structure into the second insulating layer;

opening the contact hole as far as a surface of the first  
conductive structure; and

forming in the contact hole a second conductive structure  
conductively connected to the first conductive structure.